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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,390	10/29/2003	Sang-Hyuck Ha	45982	6829

7590 10/30/2007

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	PAPER NUMBER
2112	

MAIL DATE	DELIVERY MODE
10/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,390	HA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-32* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20071025*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-19, drawn to A method for reading code symbols by deinterleaving to decode a encoder packet in a receiver for a mobile communication system supporting interleaving, wherein interim address generation step comprises the step of generating the interim address by excluding the $(J+1)^{th}$ column when the number of the code symbols of the (J+1) column is less than a half of 2^m code symbols, and generating the interim address by including the $(J+1)^{th}$ column when the number of the code symbols of the $(J+1)^{th}$ last column is more than a half of 2^m code symbols, classified in class 714, subclass 763.

II. Claims 20-27, drawn to An apparatus for reading code symbols by deinterleaving in a receiver for a communication system supporting interleaving wherein an interim address generator comprises: a first divider for outputting a maximum integer not exceeding a quotient obtained by dividing an index of a code symbol requested by the channel decoder by 2^m; a BRO operator for grouping bits obtained by dividing the code symbol index by 2^m, and performing a BRO operation on row indexes for symbols of each group; a multiplier for multiplying an output of the BRO operator by (J^{-1}); and a first adder for calculating the interim

address by adding an output of the multiplier to an output of the first divider, classified in class 714, subclass 768.

III. Claims 28-31, drawn to A method for performing addressing so as to generate deinterleaved symbols from an input buffer that performs a bit reversal order (BRO) operation on column indexes of symbols in 2^m columns among (2^mxJ+R) symbols, where 2^m is the number of columns, J is the number of columns and R is the number of remaining symbols in a $(J+1)^{th}$ column, and sequentially writes interleaved symbols corresponding to code symbol indexes k, the method comprising the steps of: performing BRO operation of column indexes of the code symbol indexes; generating a interim addresses by adding the BRO operated column indexes to a column index of the code symbol indexes; generating address compensation factor for compensating addresses of remaining symbols from the code symbol index of $(J+1)^{th}$; and generating addresses by adding the interim address values and the address compensation factors, and applying the addresses to the buffer, classified in class 714, subclass 701.

IV. Claim 32, drawn to An apparatus for performing addressing so as to generate deinterleaved symbols from an input buffer that performs a bit reversal order (BRO) operation on column indexes of symbols in 2^m columns among (2^mxJ+R) symbols, where 2^m is the number of columns, J is the number of columns and R is the number of remaining symbols in a

$(J+1)^{th}$ column, and sequentially writes interleaved symbols corresponding to code symbol indexes k, the apparatus comprising: an interim address generator for performing BRO operation of column indexes of the code symbol indexes and adding the BRO operated column indexes to a column index of the code symbol indexes; an address compensation factor calculator for generating address compensation factor for compensating addresses of remaining symbols from the code symbol index of $(J+1)^{th}$ column; and an adder for adding output of the interim address generator and output of the address compensation factor calculator, classified in class 714, subclass 702.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I to IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination Group I has separate utility such as for an interim address generation step comprises the step of generating the interim address by excluding the $(J+1)^{th}$ column when the number of the code symbols of the (J+1) column is less than a half of 2^m code symbols, and generating the interim address by including the $(J+1)^{th}$ column when the number of the code symbols of the $(J+1)^{th}$ last column is more than a half of 2^m code symbols. In the instant case, subcombination Group II has separate utility such as for an interim address generator comprises: a first divider for outputting a maximum integer not

exceeding a quotient obtained by dividing an index of a code symbol requested by the channel decoder by 2^m; a BRO operator for grouping bits obtained by dividing the code symbol index by 2^m, and performing a BRO operation on row indexes for symbols of each group; a multiplier for multiplying an output of the BRO operator by (J^{-1}); and a first adder for calculating the interim address by adding an output of the multiplier to an output of the first divider. In the instant case, subcombination Group III has separate utility such as for performing addressing so as to generate deinterleaved symbols from an input buffer that performs a bit reversal order (BRO) operation on column indexes of symbols in 2^m columns among $(2^m xJ+R)$ symbols, where 2^m is the number of columns, J is the number of columns and R is the number of remaining symbols in a $(J+1)^{th}$ column, and sequentially writes interleaved symbols corresponding to code symbol indexes k, the method comprising the steps of: performing BRO operation of column indexes of the code symbol indexes; generating a interim addresses by adding the BRO operated column indexes to a column index of the code symbol indexes; generating address compensation factor for compensating addresses of remaining symbols from the code symbol index of $(J+1)^{th}$; and generating addresses by adding the interim address values and the address compensation factors, and applying the addresses to the buffer. In the instant case, subcombination Group IV has separate utility such as performing addressing so as to generate deinterleaved symbols from an input buffer that performs a bit reversal order (BRO) operation on column indexes of symbols in 2^m columns among $(2^m xJ+R)$ symbols, where 2^m is the number of columns, J is the number of columns and R is the number of remaining symbols in a $(J+1)^{th}$ column, and

sequentially writes interleaved symbols corresponding to code symbol indexes k, the apparatus comprising: an interim address generator for performing BRO operation of column indexes of the code symbol indexes and adding the BRO operated column indexes to a column index of the code symbol indexes; an address compensation factor calculator for generating address compensation factor for compensating addresses of remaining symbols from the code symbol index of $(J+1)^{th}$ column; and an adder for adding output of the interim address generator and output of the address compensation factor calculator. See MPEP § 806.05(d).

The examiner has required restriction between subcombinations usable together. Where applicant elects a subcombination and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art due to their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

A telephone call was made to Roylance, Abrams, Berdo & Goodman, L.L.P. on 10/25/2007 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or invention to be examined even though the requirement be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention or species may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse.

Should applicant traverse on the ground that the inventions or species are not patentably distinct, applicant should submit evidence or identify such evidence now of

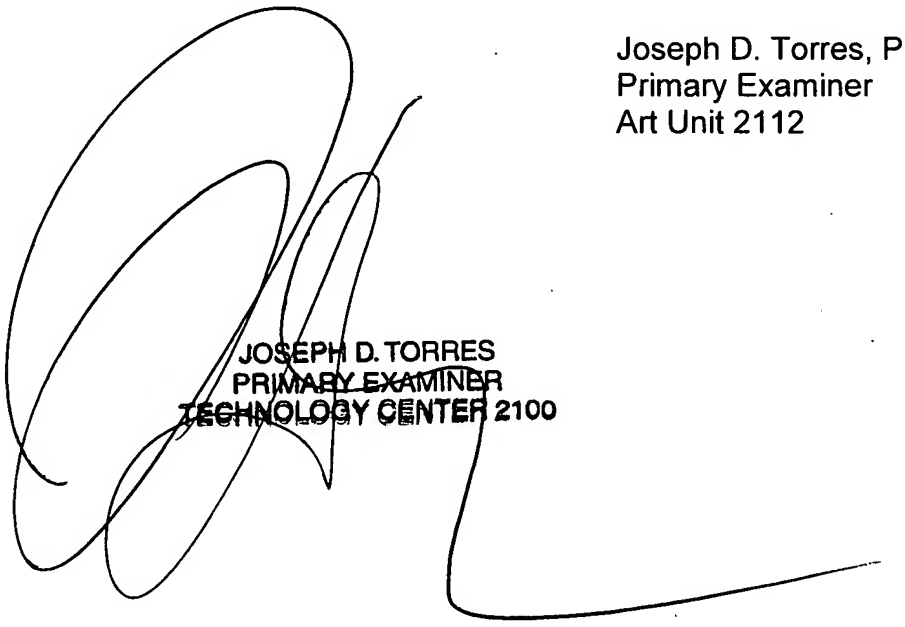
record showing the inventions or species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C.103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2112